AF/ 2631

TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. ITL.0296US

In Re Application Of: **Michael J. McTague et al.**

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JUL 25 2005
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Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/471,435	December 23, 1999	Khanh C. Tran	21906	2631	7390

Invention: **Asymmetric Digital Subscriber Loop Modem**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **June 17, 2005.**

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Dated: **July 21, 2005**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicants:	Michael J. McTague, et al.	§	Group Art Unit:	2631
Serial No.:	09/471,435	§	Examiner:	Khanh C. Tran
Filed:	December 23, 1999	§	Docket No.	ITL.0296US (P6509)
Title:	Asymmetric Digital Subscriber Loop Modem	§	Assignee:	Intel Corporation

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APPEAL BRIEF

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

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RELATED APPEALS AND INTERFERENCES

None.

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STATUS OF CLAIMS

Claims 1, 3-7, 9-15, 17-28, and 30 (Rejected).

Claims 2, 8, 16, and 29 (Canceled).

Claims 1, 3-7, 9-15, 17-28, and 30 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments have been entered.

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SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. An asymmetric digital subscriber loop modem (Fig. 1, 10) comprising:

an integrated circuit (14) (Specification at page 5, lines 4-7);

an analog-to-digital converter (20) contained in said integrated circuit (14), said converter (20) producing data at a relatively higher data rate (See Specification at page 5, lines 9-13);

a device (22) contained in said integrated circuit and coupled to said analog-to-digital converter, said device (22) reducing the higher data rate data from the analog-to-digital converter (20) to a lower data rate data (See Specification at page 5, lines 14-21);

a multiplexer (24) to multiplex said lower data rate data and control information and transmit said data and control information externally of said integrated circuit (14) (See Specification at page 5, line 22, to page 6, line 2); and

a second integrated circuit (12), said second integrated circuit (12) including a de-multiplexer (26) to de-multiplex said lower data rate data and said control information (See Specification at page 6, lines 2-5).

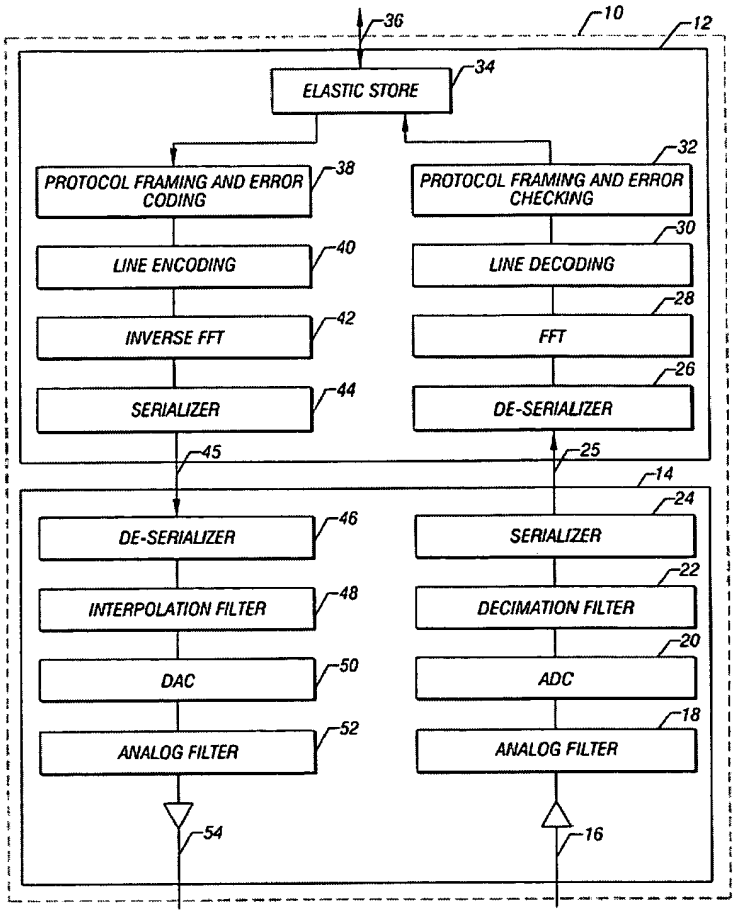

FIG. 1

12. An asymmetric digital subscriber loop modem (Fig. 1, 10) comprising:

an integrated circuit (14) (See Specification at page 5, lines 4-7);

an analog-to-digital converter (20) contained in said integrated circuit (14), said converter (20) producing data at a relatively higher data rate (See Specification at page 5, lines 9-13);

a device (22) contained in said circuit and coupled to said analog-to-digital converter, said device (22) reducing the higher data rate data from the analog-to-digital converter (20) to a lower data rate (See Specification at page 5, lines 14-21);

a multiplexer (24) to multiplex said lower data rate data and control information and transmit said data and control information externally of said integrated circuit (14) (See Specification at page 5, line 22, to page 6, line 2);

and

a second integrated circuit (12), said second integrated circuit (12) including a line encoder to produce data at a relatively higher data rate and a device coupled to said line encoder to produce data at a relatively lower data rate, said device being coupled to a serializer which transmits said data to said integrated circuit (See Specification at page 6, lines 2-5).

14. A method comprising:

receiving analog data on a first integrated circuit device (Fig. 1, 14) within a modem (10) (See Specification at page 5, lines 4-7);

converting said analog data to digital format (See Specification at page 5, lines 9-13);

decreasing the data rate of said data (See Specification at page 5, lines 14-21);

serializing said data (See Specification at page 5, line 22, to page 6, line 2);

multiplexing said serialized data with control information (See Specification at page 5, line 22, to page 6, line 2);

transmitting said data to a second integrated circuit device within the modem (See Specification at page 6, lines 2-5); and

demultiplexing said data and control information within said second integrated circuit device (See Specification at page 6, lines 2-5).

23. An asymmetric digital subscriber loop modem (Fig. 1, 10) comprising:

a first integrated circuit (14) including an analog-to-digital converter (20), a device (22) to reduce the data rate from the analog-to-digital converter to a lower data rate, and a serializer (24) to multiplex said lower data rate data with control information (See Specification at page 5, line 4, to page 6, line 2); and

a second integrated circuit (12), said serializer (24) to transmit said lower data rate data from said first integrated circuit (14) to said second integrated circuit (12), said second integrated circuit (12) including a de-serializer (26) to receive said lower data rate data from said first integrated circuit (14) and demultiplex said lower data rate data and said control information before transmitting said data to a device (28) for demodulating said data (See Specification at page 6, lines 2-13).

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

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GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. **Are Claims 1, 3-7, 9-10, 14-15, 17, 20-23, 25-26, 28, and 30 Unpatentable Over Kanekawa in View of Yukutake?**

B. **Are Claims 12-13, 24, and 27 Unpatentable Over Kanekawa and Yukutake and Further in View of Isaksson?**

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ARGUMENT

A. Are Claims 1, 3-7, 9-10, 14-15, 17, 20-23, 25-26, 28, and 30 Unpatentable Over Kanekawa in View of Yukutake?

Neither of the cited references teach a multiplexer to multiplex said lower data rate data and control information and transmit the data and control information externally of said integrated circuit.

With respect to the reference to Yukutake, it appears that the Examiner is taking the position that somehow the use of the isolators 501 and 502, in Figure 1, teach the use of separate circuits. But, even if one were to accept this relatively unusual proposition, it still fails to meet the claimed invention.

This is because there is a fundamental difference in the way the circuits in Yukutake and the claimed invention work. In the cited reference, the so-called "decimeter" 515 is apparently asserted to reduce the higher data rate. But, even if that is so, it also serializes the data. See column 7, lines 49-50. Thus, it is assumed that the device 515 is read to be the device for reducing the higher data rate in claim 1, as well as the multiplexer to multiplex said lower data rate data and control information. However, the claim further calls for a second integrated circuit which, apparently, the Examiner contends to be the stuff downstream of the isolator 502 by virtual of isolator 502 allegedly functioning as if there were a separate integrated circuit.

The problem is that the claim requires that the second integrated circuit include a demultiplexer to demultiplex the lower data rate. In the cited reference, all of the data going through the ADCR 516 in-DSP 517, RXDR 518, ex-DSP 536 and returning through the TXDR 521, in-DSP 517 is still serial data. The serial conversion is done in the DACR 522. See column 7, line 65. In other words, there does not appear to be any type of demultiplexing or de-serialization on the other side of the isolators 502 and 501 from the DCM 515 and INT 523. Thus, there is no isolation between serialized and unserialized data. All the serialized data is handled on the same side of the isolators.

In order for the analogy the Examiner is asserting to work, he would have to show that on the other side of the isolator 501, the data is de-serialized, for example, on ADCR 516. However, there is no indication that this is done in the cited reference.

Kanekawa cannot help with this deficiency since Kanekawa does not teach reducing the data rate. See the office action at page 7, lines 9-12. That is why the Examiner is relying on Yukutake.

The premise of the Examiner's position seems to be that because two references teach using a single integrated circuit with isolation devices in between regions thereof, that somehow the combination of these two references teaches using separate integrated circuits. An assertion of equivalency is not sufficient to meet the claimed invention. It does not matter whether the two circuits are functional equivalents. What matters is whether or not anything teaches what is claimed.

As explained in the Background of the present application at page 2, line 15, existing modems generally are implemented using two or more integrated circuits. One set of integrated circuits provides most of the digital signal processing and the other provides the analog to digital and digital to analog conversion. Generally, the two integrated circuits are separated after A to D conversion on the receiver side and before D to A conversion on the transmitter side. This means that data is transmitted between the two chips at relatively high data rates. This high data rate transmission results in more buffering on each chip and more pins are needed to connect the chips. This increases the cost of each chip. In addition, the high data rate results in higher system cost due to the impact of higher frequency operation and electromagnetic interference shielding.

Thus, the problem that was sought to be overcome is the one of using two separate integrated circuits, but transmitting the data between them at high data rates.

Nothing in any of the cited references suggest slowing down the data rate before transferring the data between two spaced integrated circuits. This failure of teaching makes the rejection insufficient to make out a *prima facie* rejection. Nothing has addressed the problem solved by the claimed invention. Neither of the two cited references are even faced with the same problem.

Both of the two references use a single integrated circuit as plainly depicted in their figures. The fact that they, according to the Examiner, contemplated having isolating capacitors that are separate integrated circuits is noted, but, there is no transmission between two separate integrated circuits in any of the cited references.

More poignantly, if one were to accept the Examiner's proposition that the Kanekawa reference could be effectively considered to be split in two by virtual of the circuit elements 50 and 2, along a vertical line in Figure 23, the Examiner has then presented a reference which constitutes the prior art whose problems the present invention sought to overcome. In other words, the reference shown in Figure 23 is not even as close to the present invention as what was already discussed in the Background. If one were to modify that reference with no teaching in the prior art, to make two separate circuits, all one would have would be exactly the circuit that had the very problems set forth in the Background.

The Examiner points to another reference which still does not use separate integrated circuits. Neither reference teaches a solution to the problems arising from data transfer between separate chips.

Since Yakutake used a single integrated circuit, there is nothing in Yakutake that would suggest the solution to the problems faced when separate integrated circuits are used. Whatever reason Yakutake had for decimating the data had nothing to do with the problems that arise when separate integrated circuits are provided. That is necessarily so because Yakutake did not have separate integrated circuits.

Thus, if one were to modify Kanekawa as proposed by the Examiner, he would then face all of the deficiencies noted in the Background. It seems illogical to suggest that he would appreciate the solution to those problems in a reference that does not even use two separate circuits and, therefore, does not even solve the problems.

This is merely hindsight reasoning. It is the suggestion that decimation could be used to overcome problems because a reference teaches decimation for some other purpose. There is no suggestion of using the decimation before transferring the data from one integrated circuit to another. Therefore, the fact that decimation is used before data is transferred across regions of the same integrated circuit simply does not teach a solution to the problems solved by the present invention and faced by Kanekawa.

In short, there is no teaching in any of the references or their combination of a solution to the problem only recognized by the present applicants. Therefore, the rejection should be reversed.

B. Are Claims 12-13, 24, and 27 Unpatentable Over Kanekawa and Yukutake and Further in View of Isaksson?

For the reasons set forth above, claims 12-13, 24, and 27 are patentable over the cited references.

* * *

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: July 21, 2005

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CLAIMS APPENDIX

The claims on appeal are:

1. An asymmetric digital subscriber loop modem comprising:

an integrated circuit;

an analog-to-digital converter contained in said integrated circuit, said converter producing data at a relatively higher data rate;

a device contained in said integrated circuit and coupled to said analog-to-digital converter, said device reducing the higher data rate data from the analog-to-digital converter to a lower data rate data;

a multiplexer to multiplex said lower data rate data and control information and transmit said data and control information externally of said integrated circuit; and

a second integrated circuit, said second integrated circuit including a de-multiplexer to de-multiplex said lower data rate data and said control information.

3. The modem of claim 1 wherein said device includes a decimation filter.

4. The method of claim 3 wherein said integrated circuit includes an analog filter coupled to said analog-to-digital converter in turn coupled to said decimation filter in turn coupled to said multiplexer.

5. The modem of claim 1 wherein said integrated circuit further includes a demultiplexer coupled to a device that increases the data rate of data received by said demultiplexer, said device that increases the data rate being coupled to a digital-to-analog converter.

6. The modem of claim 5 wherein said device for increasing the data rate includes an interpolation filter.

7. The modem of claim 1 wherein said integrated circuit includes both a receiver section and a transmitter section.

9. The modem of claim 1 wherein said second integrated circuit implements discrete multi-tone modulation.

10. The modem of claim 9 wherein said second integrated circuit provides digital signal processing.

11. The modem of claim 9 wherein said second integrated circuit includes a fast Fourier transformer and a line decoder.

12. An asymmetric digital subscriber loop modem comprising:

an integrated circuit;

an analog-to-digital converter contained in said integrated circuit, said converter producing data at a relatively higher data rate;

a device contained in said circuit and coupled to said analog-to-digital converter, said device reducing the higher data rate data from the analog-to-digital converter to a lower data rate;

a multiplexer to multiplex said lower data rate data and control information and transmit said data and control information externally of said integrated circuit; and

a second integrated circuit, said second integrated circuit including a line encoder to produce data at a relatively higher data rate and a device coupled to said line encoder to produce data at a relatively lower data rate, said device being coupled to a serializer which transmits said data to said integrated circuit.

13. The modem of claim 12 wherein said device is an inverse fast Fourier transformer.

14. A method comprising:

receiving analog data on a first integrated circuit device within a modem;

converting said analog data to digital format;

decreasing the data rate of said data;

serializing said data;

multiplexing said serialized data with control information;

transmitting said data to a second integrated circuit device within the modem; and

demultiplexing said data and control information within said second integrated circuit device.

15. The method of claim 14 wherein reducing the data rate of said digital data includes decimating said digital data.

17. The method of claim 14 further including receiving said data on said second integrated circuit and de-serializing said data.

18. The method of claim 17 including increasing the data rate of said data on said second integrated circuit.

19. The method of claim 18 wherein increasing said data rate includes fast fourier transforming said data.

20. The method of claim 14 further including receiving digital data for transmission by said first chip and increasing the data rate of said data.

21. The method of claim 20 wherein increasing said data rate includes interpolating said data.

22. The method of claim 21 including converting said interpolated data to an analog format signal.

23. An asymmetric digital subscriber loop modem comprising:

a first integrated circuit including an analog-to-digital converter, a device to reduce the data rate from the analog-to-digital converter to a lower data rate, and a serializer to multiplex said lower data rate data with control information; and

a second integrated circuit, said serializer to transmit said lower data rate data from said first integrated circuit to said second integrated circuit, said second integrated circuit including a de-serializer to receive said lower data rate data from said first integrated circuit and demultiplex said lower data rate data and said control information before transmitting said data to a device for demodulating said data.

24. The modem of claim 23 wherein said second integrated circuit includes a modulating circuit which decreases the data rate of digital data and a serializer which transmits said decreased data rate data to said first integrated circuit, said first integrated circuit including a de-serializer that receives said modulated data, said de-serializer coupled to a device that increases the data rate of said data, said device coupled to a digital-to-analog converter.

25. The modem of claim 23 wherein said device on said first integrated circuit for decreasing the data rate of said data is a decimation filter.

26. The modem of claim 24 wherein said device that increases the data rate on said first integrated circuit is an interpolation filter.

27. The modem of claim 24 wherein said modulating circuit includes an inverse fast Fourier transformer.

28. The modem of claim 23 wherein said modem is a splitterless remote modem.

30. The modem of claim 23 wherein lower data rate data is transmitted in two directions between said first and second integrated circuits.